OIPE IAP52 SEP 19 2005 PATENT & TRADEMARK OFFICE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Chien-Hua Chen, et al. Art Unit: 1734

Examiner: James D. Sells

Serial Number: 10/816,509

Filed: March 31, 2004

Title: SYSTEM AND METHOD FOR DIRECT-BONDING OF SUBSTRATES

Date: September 14, 2005

DECLARATION UNDER RULE 132

I, Chien-Hua Chen, do hereby declare and say:

My home address is 2214 NW Dixon Street, Corvallis, OR 97330.

I have a Master Degree in Electrical Engineer from The University of New Mexico. I have worked in the semiconductor industry about 14 years. I have been employed by Hewlett-Packard Company for about 14 years and my current position is as an R&D expert in semiconductor packaging.

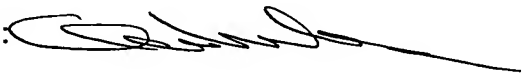
Exhibit A is a set of powerpoint slides which document experimental results of plasma bonding a glass substrate to a TEOS wafer as claimed in claim 1. Pages 1-3 describe the results when room temperature annealing. Pages 4-8 describe results when annealing at various relative low temperatures. The data contained within is believed to be a true and accurate copy of data collected during experiments performed on test devices at Hewlett-Packard facilities.

The slides exhibit the results of empirical testing of a TEOS/ TEOS plasma bond interface that were done without post-plasma wet dip of any kind. The surface energy increases quickly even under room temperature annealing (see Exhibit A, page 2 for room temp anneal and page 5 for low temp anneal). Note that the "direct bond in air" of "Room Temperature Plasma Treated SiO2/SiO2 Bonding" shown in Fig. 6A of Tong et al. (US Patent No. 6,902,987). By using the

TEOS/TEOS interface with plasma treatment and a dry-dry bond with compression without any wet treatment there is a significant amount of surface bond energy over that found in the prior art. This technique allows for sufficient surface bonding energy even with room temperature annealing to allow for optical MEMs devices that are encapsulated with a glass lid substrate to survive saw and make the packaging process practical. By avoiding any wet treatment, the optical MEMs devices are not damaged by trapped moisture which can cause stiction or fogging issues.

As shown on page 3 of Exhibit A, a 12 hr room temperature annealing provided about 400 mJ/m^2 of bond energy. After 24 hours, the bond strength increased to 500mJ/m^2. As shown on pages 4-6, by using a low temperature annealing of 100, 150, or 200 C, the annealing time can be reduced significantly to about 10 min. while increasing the surface bonding energy. In fact, as shown on pages 7-8, even at temperatures of 55, 70, or 85 C, the annealing time can be reduced to 10-20 min. and still be sufficient to survive the saw process.

I further declare that all statements made herein of my own knowledge are true an that all statements made on information and belief are believed to be true; and that these statements were mad with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patents issuing thereon.

Signed: 

Chien-hua Chen

Date: Sep 7, 2005